GENERAL DESCRIPTION

The VA1210 is a high performance, low noise differential analog MEMS voice accelerometer (a.k.a bone sensor). It features Vesper's Adaptive ZeroPower Sensing™ that dramatically extends the battery life of always-on systems. Adaptive ZeroPower Sensing™ constantly monitors the background acceleration level to activate the system when pre-configured acceleration threshold (such as the user's voice) is detected. The entire signal chain of the ZeroPower Sensing™ system is in hibernate mode while sensing for voice. When voice is detected, the accelerometer can be switched to a Normal Mode where it will operate as any standard analog low noise accelerometer. The ZeroPower Sensing™ signal chain can also be used for hardware-based Voice Activity Detect.

The VA1210 has an ultra-small 2.9 x 2.76 x 0.9mm package. The accelerometer is solder reflow compatible with no sensitivity degradation. Vesper's Piezoelectric MEMS construction also enables operation in environmentally harsh surroundings due to immunity to dust and moisture ingress protection. It is ideal for applications requiring high quality voice call in battery powered consumer devices.

FEATURES

- Adaptive ZeroPower Sensing™ (ZPS) Voice Accelerometer
- Built-in ultra-low power VAD (voice activity detection)
- Dust resistant and moisture resistant
- Differential Analog Output
- Mode selection using Mode pin
- Adaptive ZPS mode configurable through I²C
- Ultra-fast wake up (<200 µSec)
- Soft-start function to prevent pop & click noises
- BIST (Built-In-Self-Test) function
- RFI and EMI robust
- Wide Temperature Range: -40C to 85C
- Small Footprint 2.9 x 2.76mm LGA package footprint

APPLICATIONS

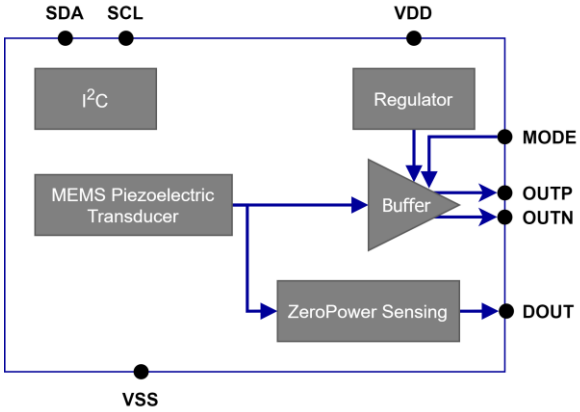
- Truly Wireless Stereo (TWS) Earbuds and Headphones
- Background Noise and Wind Noise Suppression
- Hearables
- Wearables
- Auto-Mute
- Voice Activity Detection and Tap Detection
- Surface Microphone

ORDERING INFORMATION

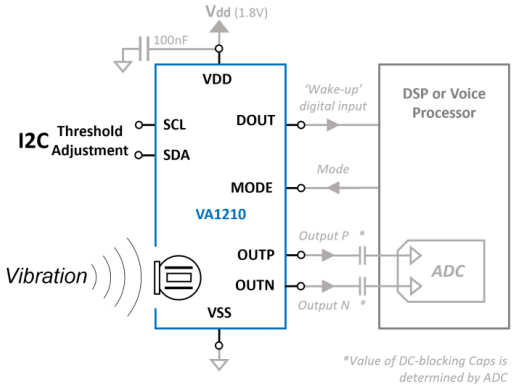
Product	Package Description	Quantity
VA1210AA	13" Tape and Reel	5,000

See Lid Marking Section for actual product marking

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



info@vespermems.com

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SPECIFICATIONS

All specifications are at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD		1.6	1.8	3.6	V
Resonance Frequency	Fr	Frequency		4		KHz
Polarity		Acceleration in +Z direction		Increase in output voltage		
Startup Time in ZPS Mode	T_{ST-ZPS}	MODE = HIGH; time taken for DOUT readiness		1		s
Startup Time Normal Mode	$T_{ST-NORM}$	MODE = LOW; time taken for OUTP/OUTN readiness		2.5		ms
Mode-Transition Time from ZPS to Normal mode (wake-up)	T_{WAKE}	Transition from ZPS mode to Normal mode within ±0.5dB of final sensitivity		200		µs
Mode-Transition Time from Normal to ZPS mode (power down)	T_{PWD}	Transition from Normal mode to ZPS mode for DOUT to be ready to trigger		10		ms
Acoustic Rejection		94dB SPL @ 250Hz, Inverse of acoustic sensitivity		85		dBV/Pa
Sensitive Axis				Z		Axis

The table below shows specifications for ZeroPower Sensing™ Mode (MODE HIGH) at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Current- ZPS Mode (1)		VDD On, MODE HIGH		10	11	µA

Note: 1) This specification table is valid for default ZPS configuration. If PGA Gain value is 0b11100 or higher, the current consumption in ZPS mode will increase from 10 µA to 15 µA

Table below shows specifications for **Normal Mode** (MODE LOW) at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output common-mode voltage	VCM			0.75		V
Output differential offset voltage	VOS			±10		mV
Output Noise		100Hz-2.4kHz, A-weighted Noise		-87		dBV(A)
Equivalent Input Noise	EIN	100Hz to 2.4kHz, A-weighted, Input Referred		0.85		mg RMS
Sensitivity	SENS	250Hz, Differential	-29	-28	-27	dBV/g
Signal-to-Noise Ratio	SNR	1g RMS @ 250Hz 100Hz-2.4kHz, A-weighted Noise		59		dB(A)
Total Harmonic Distortion	THD	1g, 250Hz		0.1		%
Max Input Level	VOP	10.0% THD		8.5		g
Power Supply Rejection Ratio	PSRR	VDD = 1.8V, 250Hz, 100mV_{PP} Sine Wave		-75		dB
Power Supply Rejection	PSR	VDD = 1.8V, 217Hz, 100mV_{PP} square wave, 100 Hz – 2.4kHz, A-weighted		-85		dB(A)
Supply Current- Normal Mode		VDD On, MODE LOW		105	115	µA
Output Impedance	ZOUT	Differential output		400		Ω

DEVICE MODES

MODE	Conditions	OUTP/OUTM Differential Output	DOUT Output	Mode Transition Time	Supply Current
OFF	VDD OFF	NA	NA	NA	NA
ZPS (1)	VDD ON, MODE HIGH	Bias only	ZPS FLAG	Normal mode to ZPS mode: 10ms	10µA (2)
Normal Mode	VDD ON, MODE LOW	Acceleration signal	ZPS FLAG	ZPS mode to normal mode: 200µs	105µA

Note: 1) The first time VDD is applied, it will take 1 second for the ZPS block, in both ZPS and Normal mode, to adapt to the environment and be ready to trigger on vibrations.
2) If PGA Gain value is 0b11100 or higher, the current consumption in ZPS mode will increase from 10 µA to 15 µA

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Supply Voltage	-0.3 to +3.6	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +150	°C
Mechanical Shock	10,000g per MIL-STD-883 M2002	

RELIABILITY SPECIFICATIONS

Stress Test	Method	Description
Temperature Cycling Test	JESD22-A104 (G)	-40°C to +125°C, 850 cycles
High Temperature Operating Life	JESD22-A108	+125°C, 1000 hours, biased
High Temperature Storage	JESD22-A103	+150C, 1000 hours, unbiased
Temperature Humidity Bias	JESD22-A101	+85°C, 85% RH, 1000 hours, biased
Reflow	J-STD-020 - Level 1	3 reflow cycles with peak temperature of +260°C
ESD-HBM	JS-001	3 discharges, all pins, ± 2kV
ESD-CDM	JS-002	3 discharges, all pins, ± 750V
Mechanical Shock	MIL-STD-883 M2002 (E)	10,000g , 0.2ms
Moisture Sensitivity Level	J-STD-020 - Level 1	Class 1

ACCELEROMETER OPERATION

VA1210 has an ultra-low power threshold-based interrupt feature referred to as ZeroPower Sensing™ (ZPS). ZPS is always running while the VA1210 is powered up. The analog output from OUTP/OUTN pins can be turned OFF and ON by controlling the MODE pin. When the application does not require the analog output, it can be turned OFF to save power consumption.

There are 2 main modes of operation for VA1210:
1. Normal mode: All functionalities of VA1210 is enabled
2. ZPS mode: Only ZPS functionality of VA1210 is enabled

The ZPS mode can be configured into 2 different sub-modes based on application needs, such as adaptive and non-adaptive ZPS modes.

NORMAL MODE

When MODE is LOW, the device enters Normal mode. VA1210 will act as a normal analog output voice accelerometer and all functionalities of VA1210 are enabled in this mode. VA1210 senses acceleration and provides a differential output on the OUTP and OUTN pins.

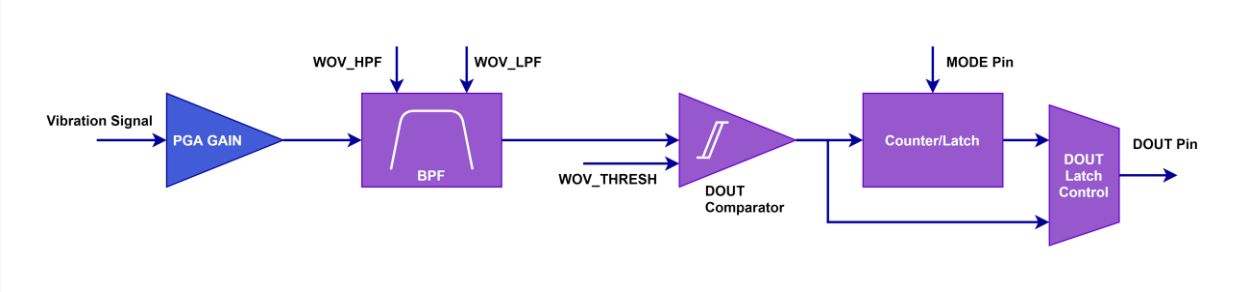
ZEROPOWER SENSING™ MODE

When MODE is HIGH, the device enters ZPS mode. There will be no output signal on the OUTP and OUTN pins, while in ZPS mode. VA1210 acts as an ultra-low power watchdog that can provide an interrupt when the input acceleration event exceeds the configured threshold. The digital output pin, DOUT, goes HIGH to indicate that the acceleration input has exceeded the set threshold. This serves as an interrupt signal to the application processor and the processor then pulls MODE line LOW to switch to Normal Mode. It is possible to configure VA1210 in adaptive and non-adaptive ZPS modes depending on application needs.

The WOV_PGA_MIN_THR and WOV_PGA_MAX_THR register values determine the ZPS mode of operation. To set VA1210 in non-adaptive ZPS mode, the WOV_PGA_MIN_THR and WOV_PGA_MAX_THR registers are set to the same value. To set VA1210 in adaptive ZPS mode, the WOV_PGA_MIN_THR and WOV_PGA_MAX_THR registers are set to different values specifying min and max threshold levels for the ZPS adaptive loop.

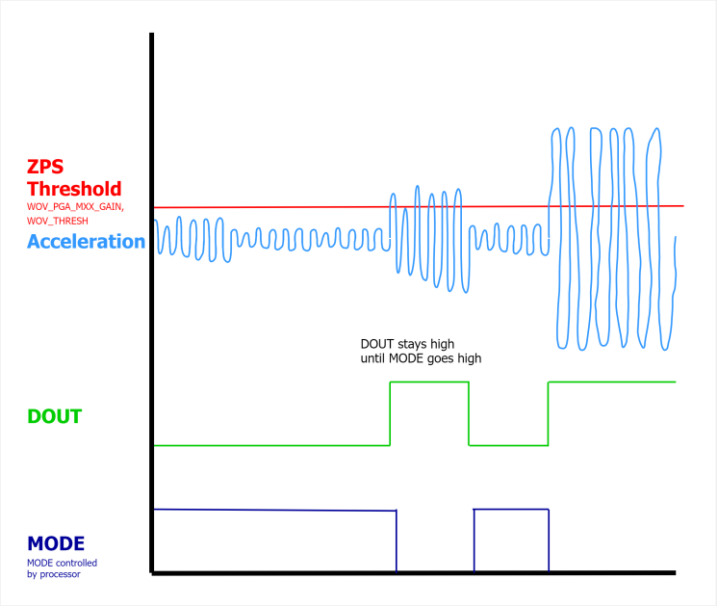
NON-ADAPTIVE ZEROPOWER SENSING™ MODE

By default, VA1210 is configured to be in non-adaptive mode. The adaptive loop is turned OFF in this case, and a simplified block diagram of the signal path is shown in the figure below. The user-programmable blocks are represented in purple. These programmable blocks can be configured by writing to the corresponding I2C registers. If the threshold detection needs to be based on an absolute acceleration level (in g RMS), then VA1210 should be configured in non-adaptive mode.



Non-adaptive Mode Block Diagram of VA1210 with I2C programmable blocks shown in purple

To set the DOUT threshold correctly in VA1210 in non-adaptive mode, it is important to understand the absolute acceleration level (in g RMS) above which the VA1210 is expected to trigger an interrupt to the processor. By default, the WOV_PGA_MIN_THR and WOV_PGA_MAX_THR values are set to 0x1B, which equates to approximately 0.013 g RMS. When intending to operate the ZPS feature of VA1210 in non-adaptive mode, it is required to set the min and max thresholds to the same value. The WOV_THRESH register then sets the trigger level multiplication factor for the value set in min/max PGA registers. The WOV_THRESH register is set to 0b000 by default, which means the triggering of DOUT will happen above 1x the threshold set in WOV_PGA_MIN_THR and WOV_PGA_MAX_THR registers, i.e, 0.013 x 1= 0.013 g RMS. If WOV_THRESH register is set to 0b001, then DOUT will trigger above 2x the threshold set by min/max PGA registers, i.e., 0.013 x 2=0.026 g RMS. To understand the default acceleration level picked up by different events in the application, it is possible to characterize the levels before finalizing the threshold settings, by recording the register value of WOV_PGA_GAIN in the application. A visual description of the VA1210 Non-adaptive ZPS mode is shown below:

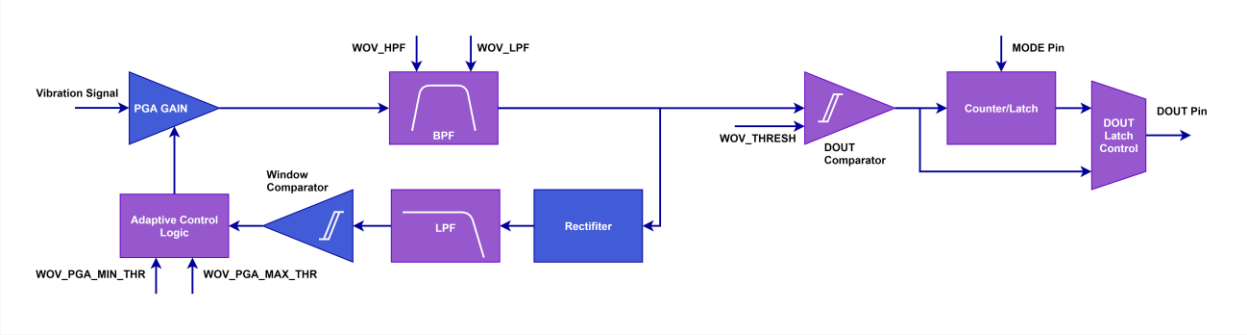


VA1210 Functional Description- Non-adaptive mode

ADAPTIVE ZEROPOWER SENSING™ MODE

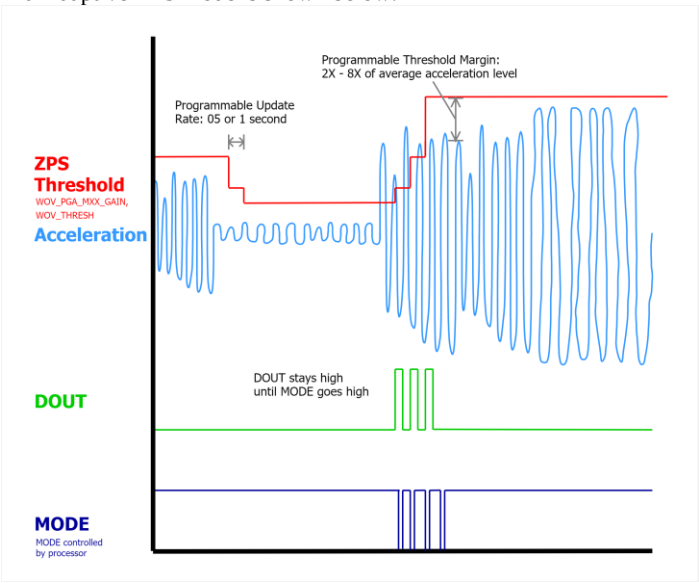
In scenarios where the environmental acceleration level changes over time and the threshold detection needs to happen, not as an absolute acceleration level in g RMS but in a relative manner, i.e., 'x' dB above or 'x' times the environmental acceleration level, then VA1210 should be configured in Adaptive ZPS mode. To set VA1210 in adaptive ZPS mode, the WOV_PGA_MIN_THR and WOV_PGA_MAX_THR registers need to be set at two different values indicating the min and max boundaries of the acceleration area of interest within which the threshold will adapt. As a good starting point, set WOV_PGA_MIN_THR to 0x0 and WOV_PGA_MAX_THR to 0x1F which utilizes the full range offered by ZPS in this mode. The WOV_THRESH register then sets the trigger level relative to the environmental acceleration level. The I2C register description section of WOV_THRESH register has more information on configuring the trigger threshold using WOV_THRESH register.

The VA1210 block diagram in adaptive mode is shown below. The blocks shown in purple indicate I2C programmable registers.



Adaptive Mode Block Diagram of VA1210 with I2C programmable blocks shown in purple

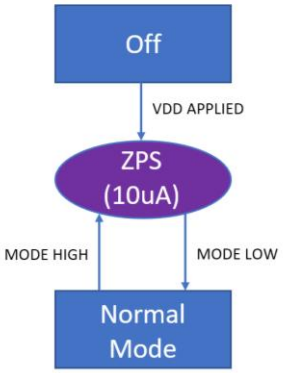
Adaptive ZPS Mode automatically senses the average acceleration level of the environment, and adjusts the gain parameter, PGA_GAIN of the programmable gain amplifier (PGA) over time. This is accomplished using a rectifier, low-pass filter (LPF), and window comparator in the feedback path of the ZPS loop as shown in above figure. This feedback path tries to keep the input of the DOUT comparator near a fixed amplitude by rectifying the signal and filtering it with a very low corner low-pass filter (configurable: 1Hz or 2Hz). Since a 1Hz or 2Hz filter is used, this gives a slow-moving, long term average representation of the input acceleration level. The adaptive loop converges to the average acceleration input level within 1 second after power up and then slows back down to either 1 Hz to 2 Hz depending on how WOV_RMS bit is set. A visual description of the VA1210 Adaptive ZPS mode is shown below:



VA1210 Functional Description- Adaptive mode

VA1210 STATE DIAGRAM

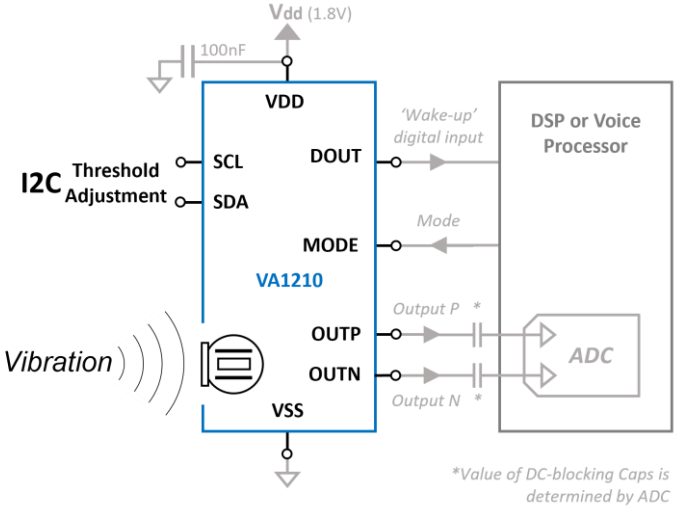
The state diagram below shows the different modes and the associated current consumption. In order to change modes, the MODE pin needs to be pulled HIGH or LOW.



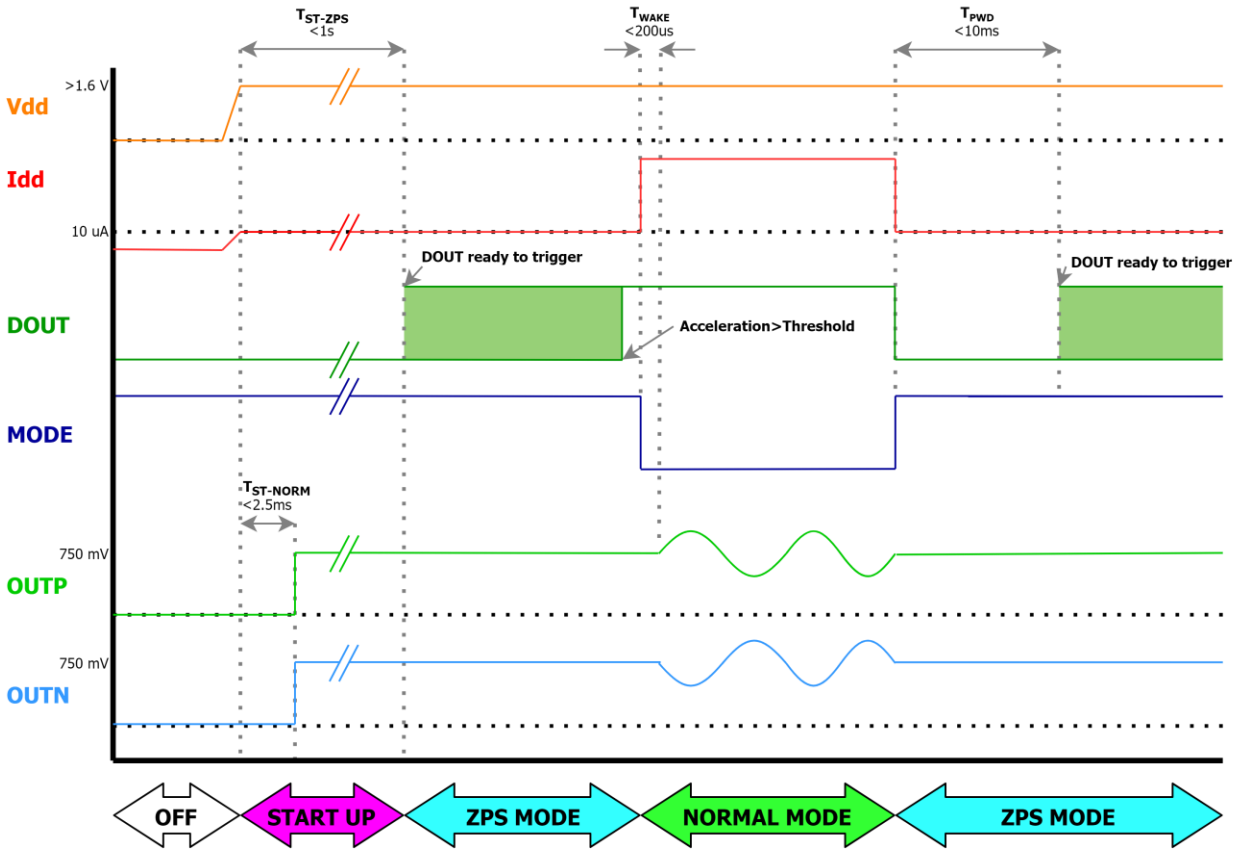
VA1210 State Diagram

SOFT START

In order to prevent any pop or click noise, the VA1210 will maintain its outputs at common mode (VCM) while in ZPS mode. This will eliminate large turn-on transients at the VA1210 outputs when transitioning from ZPS to Normal Mode.

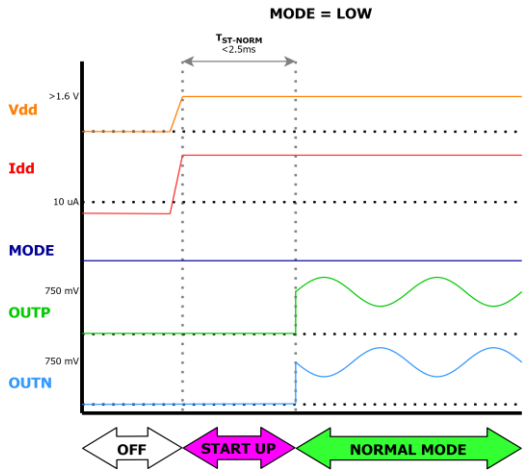


Typical Application Schematic

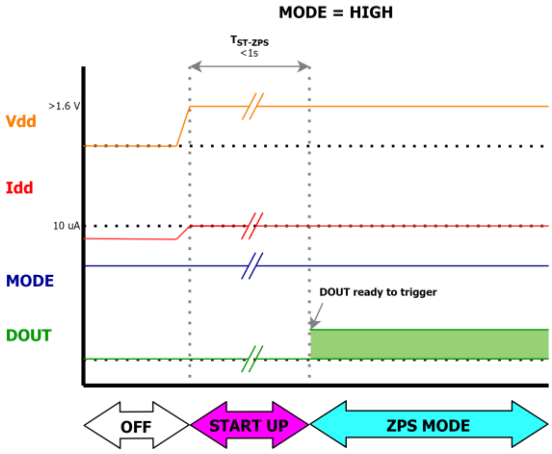


Switching between modes, when DOUT is High, the application processor can switch the VA1210 into Normal Mode. In Normal Mode, the VA1210 will output the analog audio signal.

POWER UP SEQUENCE



Power Sequence in Normal Mode



Power Sequence in ZPS Mode

The power-up sequence of VA1210 is shown in graphs above. Upon power-up, the part will enter ZPS mode if MODE is HIGH. For the first one second after power-up, the DOUT output will be blanked to allow the ZPS circuitry to power up correctly and settle. After this initial second, the DOUT pin will be free to trigger.

When MODE is applied LOW, the accelerometer will enter Normal Mode. The ZPS lineup will continue to function during Normal Mode and track the acceleration.

A DOUT pin event is not required to enter one of the accelerometer modes, anytime the MODE pin is toggled the part will transition into the required mode.

When the acceleration exceeds the ZPS threshold, the VA1210 will pull the DOUT pin HIGH, and the voice processor will have to pull the MODE pin LOW so that the VA1210 enters Normal Mode. The analog output will reach within ±0.5 dB of final sensitivity within 200µs.

Note: during ZPS mode the outputs will be held at common mode to ensure that no big DC shift will take place when transitioning to Normal Mode. This should prevent any pop or click noise.

ELECTRICAL SPECIFICATION FOR I2C

Parameter	Symbol	Conditions	Standard mode		Fast mode		Fast mode plus		Units
			Min	Max	Min	Max	Min	Max	
LOW-level input voltage [1]	V_{IL}		-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	V
HIGH-level input voltage [1]	V_{IH}		0.7 V_{DD}	[2]	0.7 V_{DD}	[2]	0.7 V_{DD} [1]	[2]	V
Hysteresis of Schmitt trigger inputs	V_{hys}				0.05 V_{DD}		0.05 V_{DD}		V
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3mA sink current; V_{DD}>2V	0	0.4	0	0.4	0	0.4	V
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2mA sink current [3]; V_{DD}<=2V			0	0.2 V_{DD}	0	0.2 V_{DD}	V

LOW-level output current	I_{OL}	V_{OL} = 0.4 V	3		3		20		mA
		V_{OL} = 0.6 V [4]			6				mA
Output fall time from V_{IHmin} to V_{ILmax}	t_{Of}			250 [5]	20 x (V_{DD} / 5.5 V) [6]	250 [5]	20 x (V_{DD} / 5.5 V) [6]	120 [7]	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}				0	50 [8]	0	50 [8]	ns
Input current each I/O pin	I_i	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	-10	+10	-10[9]	+10 [9]	-10[9]	+10 [9]	µA
Capacitance for each I/O pin [10]	C_i			10		10		10	pF

Characteristics of the SDA and SCL I/O Stages

[1] Some legacy Standard-mode devices had fixed input levels of V_{IL} = 1.5 V and V_{IH} = 3.0 V. Refer to component datasheets.
[2] Maximum $V_{IH} = V_{DD(max)}$ + 0.5 V or 5.5 V, whichever is lower. See component datasheets.
[3] The same resistor value to drive 3 mA at 3.0 V V_{DD} provides the same RC time constant when using <2 V V_{DD} with a smaller current draw.
[4] To drive a full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL}. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.
[5] The maximum t_{of} for the SDA and SCL bus lines quoted in the table below (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_{of} .
[6] Necessary to be backward compatible with fast mode.
[7] In fast-mode plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
[8] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
[9] If VDD is switched off, I/O pins of fast-mode and fast-mode plus devices must not obstruct the SDA and SCL lines.
[10] Special purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

Parameter	Symbol	Conditions	Standard mode		Fast mode		Fast mode plus		Units
			Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		0[1]	100	0	400	0	1000	kHz
hold time (repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	4.0		0.6		0.26		µS
LOW period of the SCL clock	t_{LOW}		4.7		1.3		0.5		µS
HIGH period of the SCL clock	t_{HIGH}		4.0		0.6		0.26		µS
Set-up time for a repeated START	$t_{SU;STA}$		4.7		0.6		0.26		µS
Data hold time [2]	$t_{HD;DAT}$	CBUS compatible masters	5.0						µS
		I2C bus devices	0 [3]	[4]	0 [3]	[4]	0		µS
Data set-up time	$t_{SU;DAT}$		250		100 [5]		50		ns
Rise time of both SDA and SCL signals	t_r			1000	20	300		120	ns
Fall time of both SDA and SCL Signals [3][6][7][8]	t_f			300	20 x (V_{DD} / 5.5V)	300	20 x (V_{DD} / 5.5V) [9]	120 [8]	ns
Set-up time for STOP condition	$t_{SU;STO}$		4.0		0.6		0.26		µS
Bus free time between a STOP and START condition	t_{BUF}		4.7		1.3		0.5		µS
Capacitive load for each bus line [10]	C_b			400		400		550	pF
Data valid time [11]	$t_{VD;DAT}$			3.45 [4]		0.9 [4]		0.45 [4]	µS

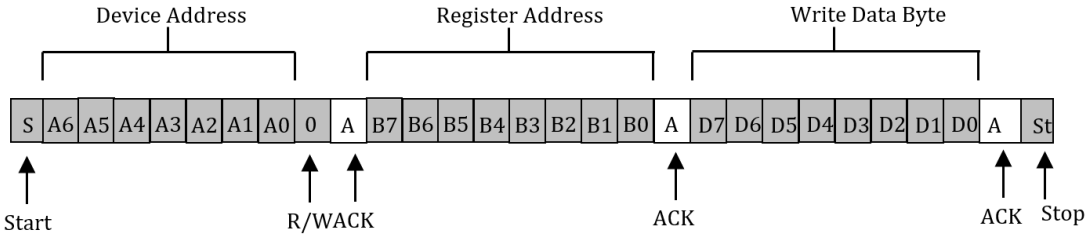
Data valid acknowledge time [12]	$t_{VD;ACK}$			3.45 [4]		0.9 [4]		0.45 [4]	µS
Noise margin at the LOW level	V_{nL}	For each connected device (including hysteresis)	0.1 V_{DD}		0.1 V_{DD}		0.1 V_{DD}		V
Noise margin at the HIGH level	V_{nH}	For each connected device (including hysteresis)	0.2 V_{DD}		0.2 V_{DD}		0.2 V_{DD}		V

Characteristics of the SDA and SCL bus lines for Standard, Fast, Fast mode plus I2C bus devices

[1] f_{SCL} = Min frequency of SCL of 0 assumes the WDT is disabled
[2] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission, and the acknowledge.
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[4] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
[5] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also, the acknowledge timing must meet this set-up time.
[6] If mixed with Hs-mode devices, faster fall times according to the table are allowed.
[7] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[8] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
[9] Necessary to be backward compatible to Fast mode.
[10] The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.
[11] $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
[12] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse)

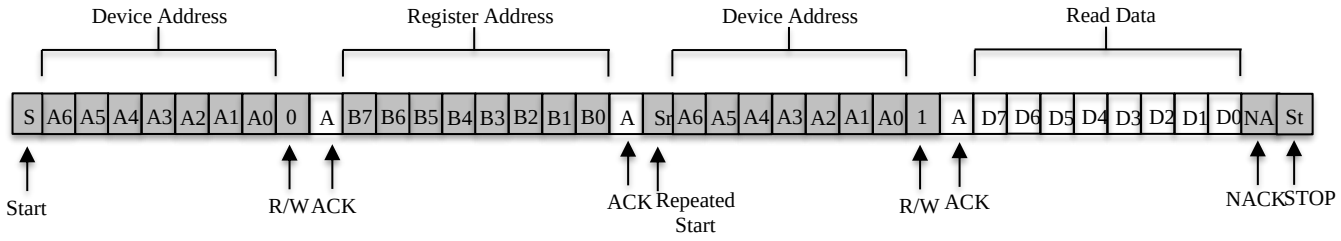
I2C TRANSACTIONS

The I2C write transaction is show below. The device address is transmitted first followed by the Read/Write (R/W) bit, to determine whether the transaction is a read or write transaction followed by the register address and the write data. The 7 bit device address is made up of 7 hard coded bits, A6 thru A0, that are hard coded to 61 hex. In the case of the I2C write transaction the R/W bit is low. The ACK is transmitted by the VA1210's I2C interface by pulling the SDA pin low.



I^2C Write Transaction

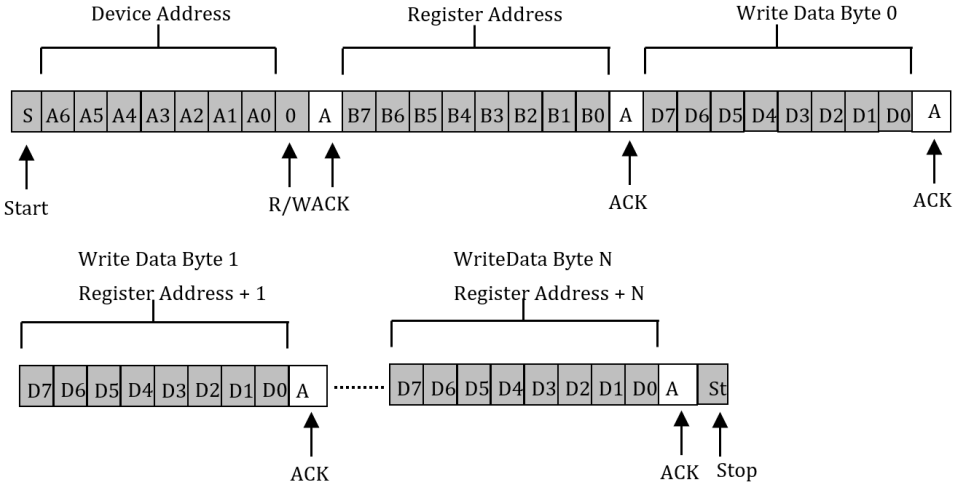
The I2C read transaction starts out the same as the write transaction with device address followed by R/W bit low followed by the register address. The difference is after the register address a repeated start condition is issued following by the device address again. After the device address the R/W bit is transmitted high. Once the I2C slave sees the R/W bit high, the I2C slave will start transmitting the 8 bit data from the register selected by the register address. To end the read transaction the I2C master will issue a NACK followed by a STOP.



I²C Read Transaction

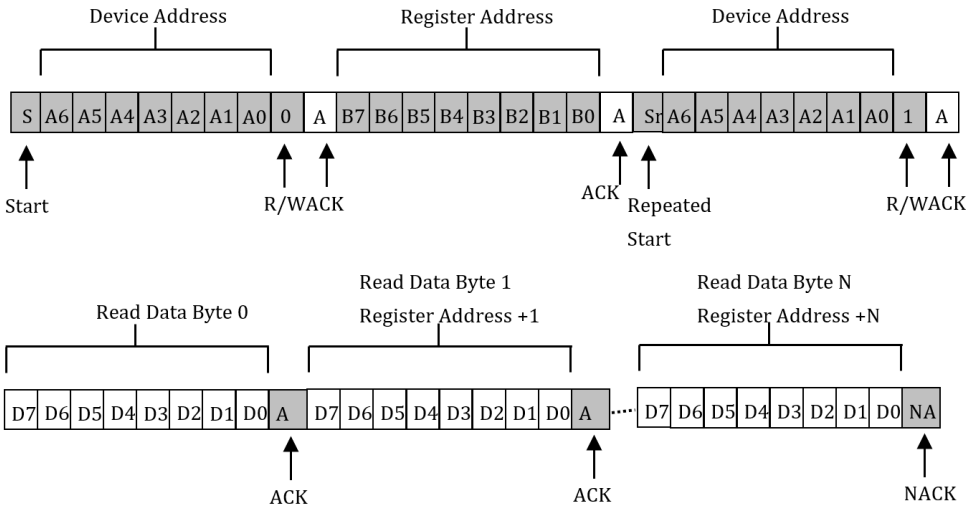
EXTENDED I2C TRANSACTION

The I2C Interface supports extended read and write transactions of the registers. The write burst transaction shown below starts out as a normal I2C write except instead of issuing a Stop at the end of the transaction, the transaction continues. As each byte is written the register address is incremented to write the next byte. The burst is finally ended by issuing a Stop following the last written byte.



I²C Write Burst

The read burst starts out with a I2C Read transaction as shown below. At the end of the first byte read by the I2C Master the I2C Master issues an ACK instead of a NAK. As each byte is read back by the I2C Master, the register address is incremented to the next register to be read. The read burst transaction is finally ended by a NACK followed by a STOP.



I²C Read Burst

I2C ADDRESS

The VA1210 has one I2C address; 0x61.

I2C REGISTERS

The I2C Registers below are user-programmable by setting the appropriate register settings.

Values in parenthesis indicate the default settings for I2C registers shipped with the device. These default values can be read back from the device using I2C readback. The 'WOV' acronym in the register and bit-field names refers to 'Wake on Vibration', or in other terms, Zero Power Sensing™..

Feature	Address	B7	B6	B5	B4	B3	B2	B1	B0	Read/Write
I2C_Cntrl	0x0			MODE (0x0)	DOUT_CLEAR (0x0)	DOUT_RAW (0x0)	WDT_DLY (0x0)		WDT_ENABLE (0x0)	R/W
WOV_PGA_GAIN	0x1				WOV_PGA_GAIN					R
WOV Filter	0x2				WOV_HPF (0x0)		WOV_LFP (0x0)			R/W
WOV PGA MIN THR	0x3		FAST_MODE_CNT (0x0)		WOV_PGA_MIN_THR (0x1B)					R/W
WOV PGA MAX THR	0x4			WOV_RMS (0x0)	WOV_PGA_MAX_THR (0x1B)					R/W
WOV THRESH	0x5						WOV_THRESH (0x0)			R/W
BIST Cntrl	0x6							BIST_POL (0x0)	BIST_EN (0x0)	R/W

User Programmable I2C Registers

I2C USER PROGRAMMABLE REGISTERS IN VA1210

MODE: this bit will act like the MODE pin if the MODE pin is kept LOW. When this bit is set at 0 the VA1210 will be in Normal Mode. When this bit is set at 1 the VA1210 will be in ZPS mode.

DOUT_CLEAR: when set to 1, DOUT pin will be reset to LOW. This is another way to reset the ZPS mode to look for acceleration trigger without toggling the MODE pin. The DOUT_CLEAR bit will reset to zero after the DOUT pin goes low.

DOUT_RAW: when set to 1, DOUT pin will be set as a raw mode which will give access to the DOUT comparator output. When DOUT_RAW is set at 0 the output will be latched until the MODE pin is pulled high again. When set to 1 the DOUT pin can be used to determine when voice is detected and goes above a preset threshold. This function can be used as a Hardware VAD function.

Note: based on Vesper's internal analysis the Hardware VAD function will perform best if WOV_PGA_MIN_THR and WOV_PGA_MAX_THR are set to the same value at 0x1B. This will ensure that the ZPS loop stops adapting. The WOV_THRESH is programmed at 0x0 by default but a value of 0x1 can also be used. It is recommended to try the VAD function on multiple users before choosing the final parameters of the ZPS lineup.

WDT_Delay: In the rare case when the host stops toggling the SCL clock in the middle of an I2C transaction, I2C interface has a Watch Dog Timer to reset the I2C logic. By default, the timer is reset and disabled upon detection of either SCL or SDA transaction. If the timer exceeds the time controlled by the WDT_DLY bits, then the entire I2C logic is reset (the registers and all other logic on VA1210 are not affected). **WDT_Delay** register Sets the watchdog time delay.

WDT_DLY (0b)	Watchdog Timer Delay (ms)
00	8
01	16
10	32
11	64

WDT_Enable: The Watchdog Timer can be disabled by setting the WDT_ENABLE bit low.

PGA Gain (WOV_PGA_GAIN): The PGA gain value represents the current input acceleration level. VA1210 can continuously monitor the acceleration level to make decisions at the application level as well as to characterize acceleration levels in different applications for specific events. The PGA Gain can be read back from the PGA_GAIN I2C register in both Normal and ZPS modes of operation. The table below shows how to convert the PGA gain values read back from the device to a real world acceleration value in g RMS.

WOV_PGA_GAIN, WOV_PGA_x_THR (0b)	Acceleration (g RMS)	WOV_PGA_GAIN, WOV_PGA_x_THR (0b)	Acceleration (g RMS)
00000	1.3	**10000**	0.08
00001	1.1	**10001**	0.07
00010	0.9	**10010**	0.06
00011	0.8	**10011**	0.05
00100	0.7	**10100**	0.042
00101	0.6	**10101**	0.036
00110	0.5	**10110**	0.030
00111	0.4	**10111**	0.025
01000	0.34	**11000**	0.021
01001	0.28	**11001**	0.018
01010	0.24	**11010**	0.015
01011	0.20	**11011 (default)**	0.013
01100	0.17	**11100**	0.011
01101	0.14	**11101**	0.009
01110	0.12	**11110**	0.008
01111	0.10	**11111**	0.006

Look up table for PGA gain values and PGA min and max threshold values

PGA min and max threshold registers (WOV_PGA_MIN_THR, WOV_PGA_MAX_THR): The PGA min and max threshold registers can be used to set VA1210 in adaptive ZPS mode or non-adaptive ZPS mode. Their register setting also controls the threshold trigger level in combination with WOV_THRESH register. The table above, showing PGA gain relationship to acceleration in g RMS, also serves as a look up table for WOV_PGA_MIN_THR and WOV_PGA_MAX_THR registers. When in non-adaptive mode, min and max thresholds are set at the same value, for example, 0x1B, which is the default setting. When in adaptive mode, the min and max thresholds are different covering the range over which the threshold adaptation should take place.

Note: The above look up table values for min and max PGA thresholds are valid for WOV_THRESH of 0x000. The WOV_THRESH register description has more details on how to comprehend actual threshold levels based on WOV_THRESH values and if VA1210 is in adaptive or non-adaptive ZPS mode.

Band Pass Filter (BPF) can be programmed via I2C to adjust the lower and upper frequency between which the device will wake up. The corner frequency settings supported by WOV_LPF and WOV_HPF register bits are below:

WOV_LPF (0b)	Corner Frequency (kHz)
000	1
100	2
101	4
110	6
111	8

Low-pass Filter Corners (Address 0x2, Bitfield: [2:0])

WOV_HPF (0b)	Corner Frequency (Hz)
00	200
01	300
10	400
11	800

High-pass Filter Corners (Address 0x2, Bitfield: [4:3])

FAST_MODE_COUNT can be programmed to increase the speed at which the ZPS feedback loop adapts to a large change in background noise. The FAST MODE is triggered according to the FAST_MODE_CNT setting described in the table below. For example, when FAST_MODE_CNT[1:0]=01, if the PGA Gain is incremented two times in a row or decremented two times in a row, the FAST MODE will engage. This setting gets enforced only on a temporary basis until the loop settles to a stable value and after that point, the refresh rate reverts back to 1Hz or 2Hz based on WOV_RMS value.

FAST_MODE_CNT[1:0] (0b)	Description
00	Fast mode disabled
01	If two window comparator trips in a row in the same direction, the clocks are sped up 16x
10	If four window comparator trips in a row in the same direction, the clocks are sped up 16x
11	If six window comparator trips in a row in the same direction, the clocks are sped up 16x

Adaptive Loop Fast Start Count (Address 0x3, Bitfield: [6:5])

WOV_RMS can be set to Low (0b0) or High (0b1) to switch the sampling interval of the comparator signal between 1 second and 0.5 second. This effectively changes the low pass corner frequency from 1Hz to 2Hz.

WOV_RMS (0b)	Comparator Sampling Interval (seconds)
0	1
1	0.5

Adaptive Loop Update Frequency (Address 0x4, Bitfield: [5])

WOV_THRESH sets the threshold level that the input acceleration signal must exceed to trigger DOUT pin HIGH.

In non-adaptive ZPS mode, WOV_THRESH value sets the multiplier for the absolute acceleration trigger level set by WOV_PGA_MIN_THR and WOV_PGA_MAX_THR values. For example, if WOV_THRESH is set to 0b100 and WOV_PGA_MIN_THR and WOV_PGA_MAX_THR are set to their default value 0x1B (0.013 g RMS), then the DOUT will trigger when input absolute acceleration level exceeds 5x 0.013 g RMS, i.e., 0.065 g RMS.

In adaptive mode, WOV_THRESH sets the amount of margin above the RMS background acceleration level that is needed to trip the DOUT pin. For example, WOV_THRESH value of 0b100 will program the accelerometer to trigger at a level 5x (or 14dB) above the RMS background acceleration level.

The table below outlines the different WOV_THRESH values available and what they represent in adaptive and non-adaptive modes.

WOV_THRESH (0b)	NON-ADAPTIVE MODE Trigger input level multiplier for WOV_PGA_x_THR register values	ADAPTIVE MODE Trigger input level relative to average acceleration noise level
000	1x (Default)	Reserved/ See note below
001	2x	6dB (2x)
010	3x	9.5dB (3x)
011	4x	12dB (4x)
100	5x	14dB (5x)
101	6x	15.5dB (6x)
110	7x	16.9dB (7x)
111	8x	18dB (8x)

Dout Comparator Threshold Programmable Values

Note: WOV_THRESH value of 0b000 is not recommended for VA1210 when in adaptive ZPS mode. This setting corresponds to DOUT going HIGH when the input acceleration signal is 1x above the background acceleration noise level. Therefore, DOUT will trip often just from fluctuations in input acceleration level, and the accelerometer may trigger consistently.

BIST_EN and **BIST_POL**: VA1210 has a BIST function to help the customer test the VA1210 during manufacturing. To enable this function the BIST_EN bit needs to be set to 1. The BIST_POL controls the polarity of the test.

BUILT-IN SELF-TEST (BIST)

Built-In Self-Test (BIST) is a self-test feature which makes it easy to check the health of the VA1210 device and its analog connections (e.g. to the ADC). BIST makes it possible to test the VA1210 in mass-production without using expensive test equipment such as a shaker.

BIST involves two tests, referred to as Test 0 and Test 1. The results from these two tests determine if the VA1210 is working correctly.

To perform BIST Test 0:

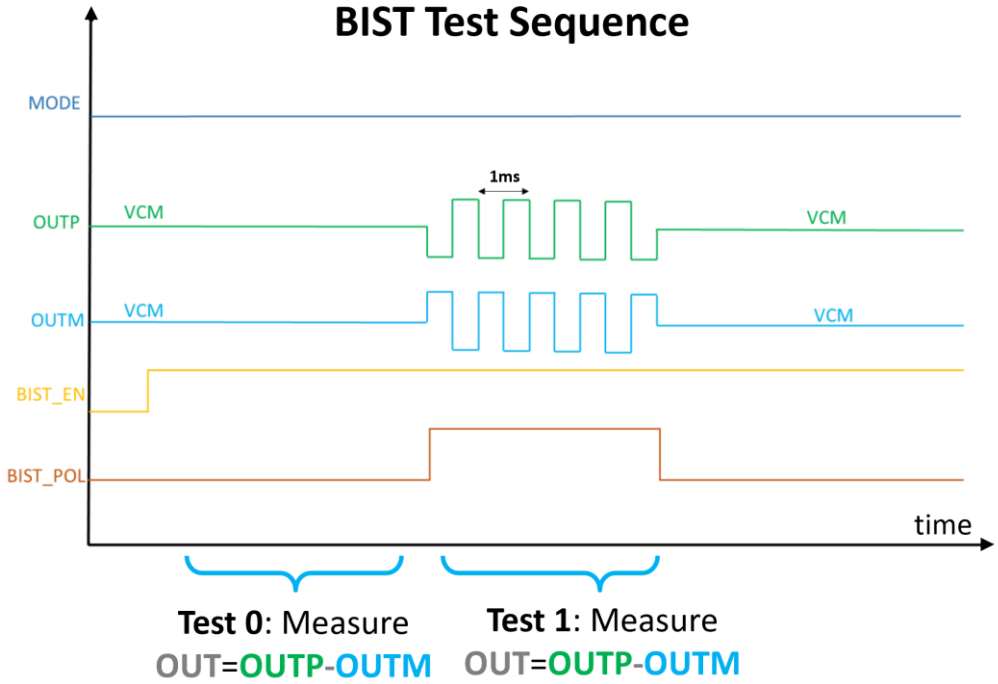
1. Set MODE pin LOW
2. Write 0x1 to Register 0x6 (BIST_POL = 0, BIST_EN = 1)
3. Measure the RMS value of the output signal (OUT = OUTP - OUTM)
    a. Ignore DC bias. Calculate RMS value of the AC-coupled signal.

To perform BIST Test 1:

1. Set MODE pin LOW
2. Write 0x3 to Register 0x6 (BIST_POL = 1, BIST_EN = 1)
3. Measure the RMS value of the output signal (OUT = OUTP - OUTM)
    a. Ignore DC bias. Calculate RMS value of the AC-coupled signal.

To exit BIST mode:

1. Write 0x0 to Register 0x6 (BIST_POL = 0, BIST_EN = 0)



BIST expected test waveform. See "BIST expected value table" for OUT threshold.

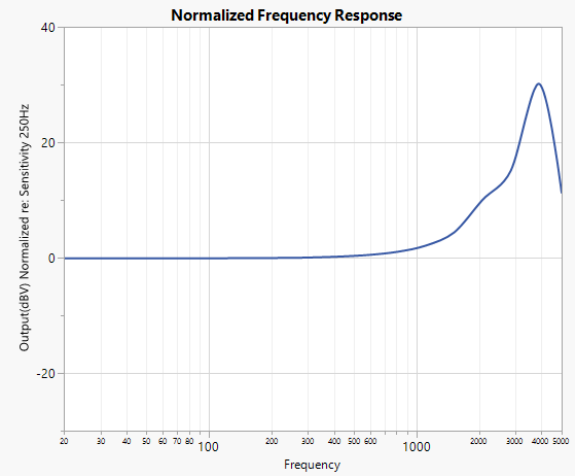
The amplitude of the output signals measured during BIST Test 0 and Test 1 will determine the result of the test. When measuring the amplitude of the signal, ignore the DC bias and calculate the RMS value of the AC-coupled signals in each case and compare against the table below to determine if the system is healthy.

RESULT OF TEST 0	RESULT OF TEST 1	INTERPRETATION
Small square wave (**OUT** < 10mVrms)	Large square wave (**OUT** > 150mVrms)	**System is healthy**
Small square wave (**OUT** < 10mVrms)	Small square wave (**OUT** < 150mVrms)	System is not healthy; Most likely an electrical issue
Large square wave (**OUT** > 10mVrms)	Large square wave (**OUT** > 150mVrms)	System is not healthy; Most likely a mechanical issue
Large square wave (**OUT** > 10mVrms)	Small square wave (**OUT** < 150mVrms)	

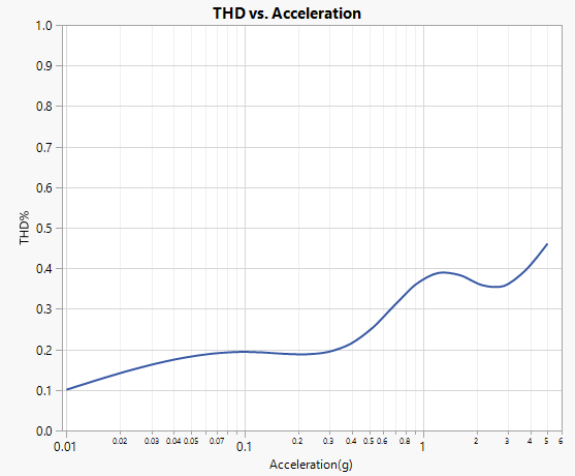
BIST expected values table

The BIST functionality relies on MEMS being still during the test. If there is any external vibration coupling into the MEMS during the BIST test, it can cause false acceptance or rejection of VA1210.

TYPICAL PERFORMANCE CHARACTERISTICS

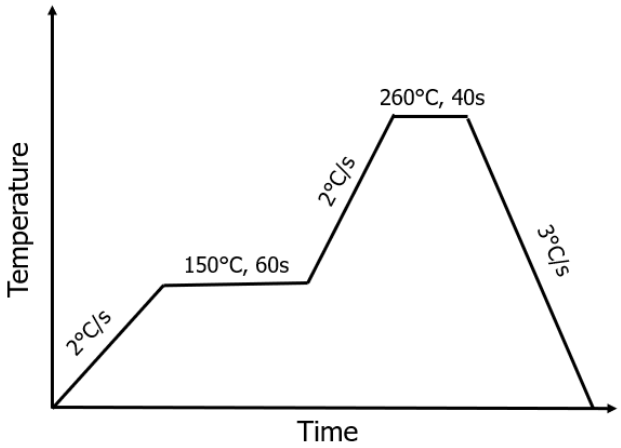


Normalized Frequency Response



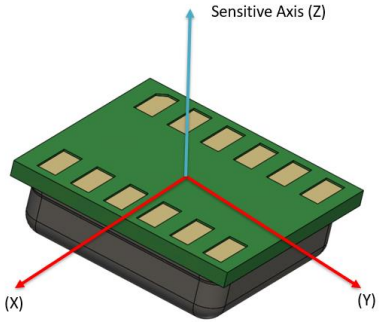
THD (%) vs Acceleration (g)

SOLDER REFLOW PROFILE



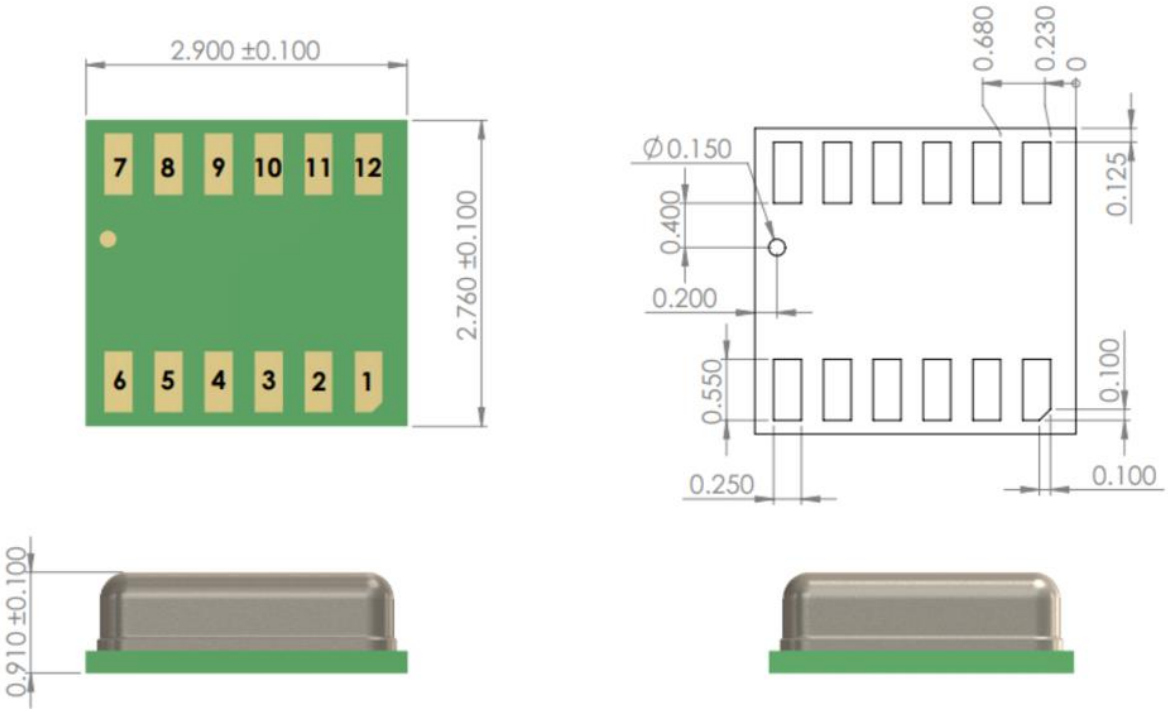
Solder Reflow Profile

SENSITIVE AXIS



Note: Sensitive Axis (Z), Direction Shown (Z-)

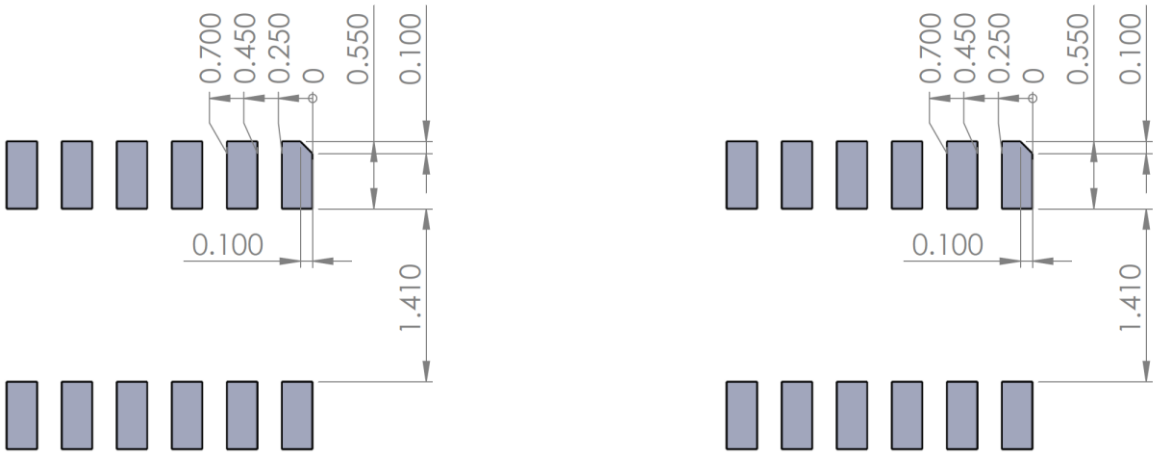
DIMENSIONS AND PIN LAYOUT (Bottom View / Terminal Side Up)



(All dimensions are in mm)

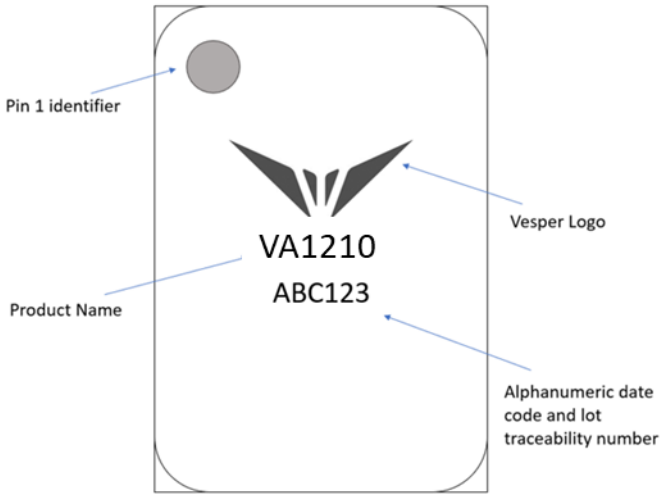
Pin Number	Pin Name	Functionality
1	OUTP	Positive Analog Output
2	OUTN	Negative Analog Output
3	GND	Ground
4	SDA	I2C Data
5	SCL	I2C Clock
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	MODE	Mode pin to change VA1210 mode of operation
11	DOUT	DOUT interrupt
12	VDD	Power

PCB DESIGN AND LAND PATTERN LAYOUT (Top View / Terminal Side Down)



PCB and Solder Stencil Pattern – All dimensions are in mm

LID MARKING



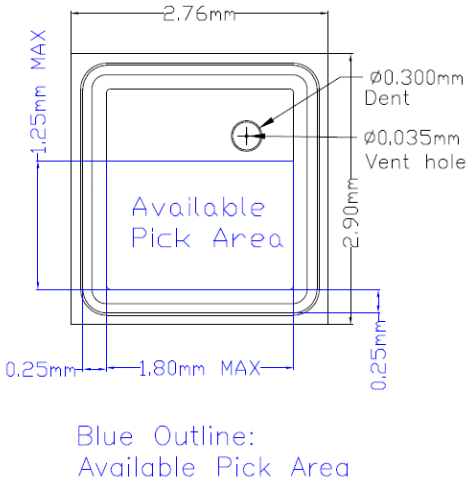
Lid Marking Description

Note: Parts marked "VE" in the product name are Engineering samples. Final samples will be marked "VA"

HANDLING INSTRUCTIONS

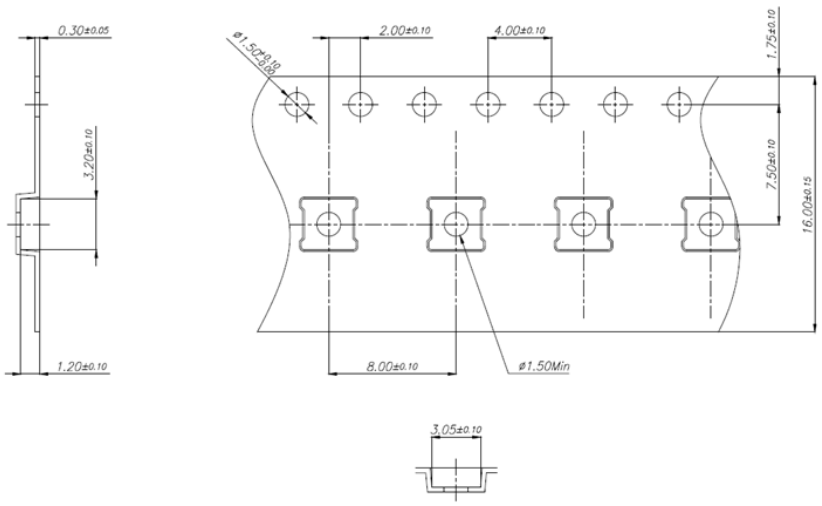
Vesper's piezoelectric MEMS devices are very resistant to harsh environments such as dust and moisture. However, to avoid mechanical damage to the MEMS structure, we recommend using appropriate handling procedures when manually handling the parts or when using pick and place equipment. The following guidelines will avoid damage:

- Do not board wash or clean after the reflow process.
- Use a placement force of <1,000g when using a pick and place machine.
- Recommended device pick location is given below

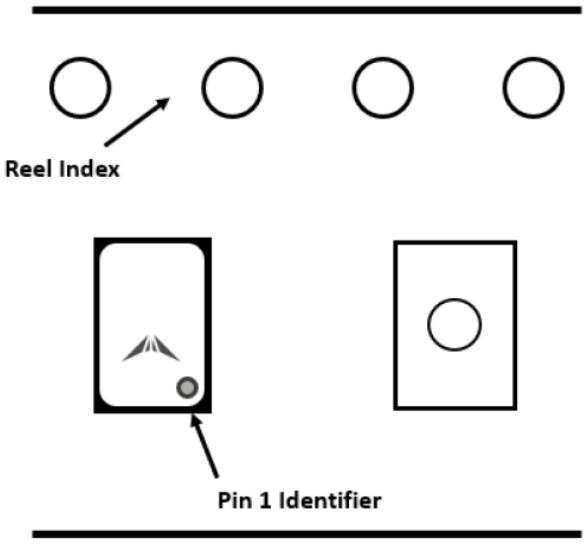


Recommended device pick location

TAPE AND REEL SPECIFICATIONS



Tape & Reel specification



Part Orientation in Reel (dimension not to scale)

SUPPORTING DOCUMENTS

AN10 – Vesper Piezoelectric MEMS Voice accelerometers Assembly and Handling Guideline
AN12 – Vesper Piezoelectric MEMS Voice Accelerometers DESIGN GUIDELINES
Technical Paper - VA1200 - Signal Validation Procedures
Migration from VA1200 to VA1210
VA1210- SELF TEST (BIST) Explanation
Flex-Board VA1210 – User Guideline

COMPLIANCE INFORMATION

Electrostatic discharge (ESD) sensitive device:
Although this product features industry-standard protection circuitry, damage may occur if subjected to excessive ESD. Proper ESD precautions should be taken to avoid damage to the device.

CONTACT DETAILS

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LEGAL INFORMATION

For any questions or comments on the datasheet email: erratum@vespermems.com

REVISION HISTORY

Revision	Date	Description
0.0.0	03/07/2022	Initial Revision
0.0.1	07/15/2022	Updated description of BIST and ZeroPower Sensing™ features; minor clarifications & formatting changes